EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Yipeng Li on May 23, 2008.

The application has been amended as follows:

In the claims:

1. (currently amended) An apparatus, comprising:

control logic comprising a plurality of logic cells, at least one of the plurality of logic cells configured to receive an A operand and a B operand and perform the following logic operations comprising $\overline{A}$ B, A$\overline{B}$, and AB; and

switch circuitry coupled to receive input data, the switch circuitry coupled to the control logic to receive a result of the AB logic operation from each of the plurality of logic cells and selectively enable the output of one or more bits of the input data based on the results of the AB logic operations;

wherein the control logic is coupled to receive a first plurality of enable signals, each of the first plurality of enable signals corresponding to a first plurality of one or more bits of a first segment of the input data, and wherein the control logic is coupled to receive a second plurality of enable signals, each of the second plurality of enable

signals corresponding to a second plurality of one or more bits of a second segment of the input data.

Cancel claim 2.

In claim 3 at line 1, delete “2” and replace with “1”.

In claim 6 at line 1, delete “2” and replace with “1”.

11. (currently amended) An apparatus, comprising:

control logic comprising a plurality of logic cells, at least one of the plurality of logic cells configured to receive an A operand and a B operand and perform the following logic operations comprising $\overline{A}$ B, A$\overline{B}$, and AB; and

switch circuitry coupled to receive input data, the switch circuitry coupled to the control logic to receive a result of the AB logic operation from each of the plurality of logic cells and selectively enable the output of one or more bits of the input data based on the results of the AB logic operations;

~~The apparatus of claim I, further comprising:~~

a content addressable memory (CAM) array coupled to receive ~~the~~ a comparand; and

a filter circuit coupled to the CAM array, the filter circuit comprising the switch circuitry and the control logic, wherein the filter circuit is coupled to receive the input data and transpose the one or more bits of the input data from an initial position in the input data to a different position in the comparand relative to other bits of the input data that are transposed to the comparand.

14. (currently amended) An apparatus, comprising:

control logic comprising a plurality of logic cells, at least one of the plurality of logic cells configured to receive an A operand and a B operand and perform the following logic operations comprising $\overline{A}$ B, A$\overline{B}$, and AB; and

switch circuitry coupled to receive input data, the switch circuitry coupled to the control logic to receive a result of the AB logic operation from each of the plurality of logic cells and selectively enable the output of one or more bits of the input data based on the results of the AB logic operations;

~~The apparatus of claim I,~~

wherein at least another of the plurality of logic cells is configured to receive a result of the $\overline{A}$ B logic operation of the at least one logic cell and an enable signal as the B operand, and wherein the at least another of the plurality of logic cells is configured to perform the AB logic operation.

Cancel claims 26-30, 32, and 34-35.

Allowable Subject Matter

2. Claims 1, 3-15, and 17-24 are allowed.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J. Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Gary J Portka/
Primary Examiner, Art Unit 2188
May 26, 2008